Theory and Analysis of GaAs MESFET Mixers

STEPHEN A. MAAS

Abstract—**A generalized analysis of the GaAs MESFET mixer is presented. Its advantage is that many of the simplifying assumptions in previous approaches have been substantially eliminated. Using this approach, the nonlinearities of any number of elements in the FET equivalent circuit may be included, any number of local oscillator (LO) harmonics and mixing products may be considered, unusual mixers such as subharmonic mixers, upconverters, and mixers with high IF frequencies can be analyzed.**

The theory has been verified experimentally. Two mixers are described: one exhibits 11.5-dB conversion gain with +9-dBm LO power, 5.6-dB minimum noise figure and +15-dBm third-order intermodulation intercept, and another which exhibits 500-MHz bandwidth, 6-dB minimum gain, 5.5-dB maximum noise figure, and +12-dBm third-order intercept at +6-dBm LO power.

I. Introduction

Although in recent years there has been great interest in the analysis and modeling of resistive (diode) mixers, a general approach to the analysis of GaAs MESFET mixers has not yet been presented. This situation is surprising in view of the rapid progress in GaAs MESFET amplifier and monolithic circuit applications. FET mixers have important applications in monolithic circuits for small, low-cost communications receivers and in more conventional microwave hybrids for compact high-performance spacecraft receivers. The purpose of this study is to develop an analysis of FET mixers which, for the purpose of predicting conversion performance, is as useful as those developed for diode mixers.

Earlier attempts to analyze FET mixers have been of limited accuracy or applicability; usually the FET equivalent circuit is simplified, the effects of higher order mixing products or local oscillator (LO) harmonics are ignored, or the effects of nonlinear elements other than the transconductance are not considered. Pucel *et al.* [1] assume a very simple lumped-element model of the FET, where only the transconductance is assumed to be nonlinear, and terminations at the signal frequency, LO fundamental, image, and IF are considered. The gate–drain capacitance and source inductance, important feedback elements, are neglected. Ntake [2] uses a similar approach but includes the effect of fixed gate–drain capacitance. He includes a very approximate noise analysis, which shows moderate experimental agreement. Harrop [3] analyzed the FET mixer using a general-purpose Volterra series computer program. This approach does not require such severe limitations on the FET lumped model, but his program is limited to fourth-order mixing products. Kurita and Morita [4] approach the problem by considering mixing in the gate–channel Schottky-barrier junction. This analysis is also approximate and applies to a mode of operation, forward-biasing the gate junction, which does not give optimum performance and is unacceptable for high-reliability applications. Begemann extends [1] to the case of a drain mixer [5]. In another paper [6], he presents a Y-parameter formulation which assumes that the parameter Y_{21} is real but nonlinear, and that the other Y parameters are the same for nonlinear operation as linear.

The assumptions shared by these analyses limit their application to downconverters with low IF frequencies. They are not applicable to harmonic mixers, upconverters, and, except for [5], mixers with the LO applied to the drain. Since feedback elements in many cases are ignored, they do not predict stability or input–output impedances. Finally, the effects of nonlinear elements other than transconductance, especially R_{ds}, are often substantial and generally can not be ignored.

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The author is with the University of California, Los Angeles, and TRW Electronic Systems Group, Redondo Beach, CA 90278.

II. Theory

The equivalent circuit of Fig. 1 can be used as an incremental large-signal model for the FET. The values of the circuit elements and their voltage or current dependencies can be determined from S parameters measured at different bias voltages, or from an analytical FET model. Under large-signal LO excitation, the source and load networks must satisfy the frequency-domain relations

$$V_{sn} - Z_{sn}I_{sn} - V_{gsn} = 0 \tag{1}$$

$$V_{Ln} - Z_{Ln}I_{Ln} - V_{dsn} = 0$$

$$n = 0,1,2,3,\cdots \tag{2}$$

where the terms represent the nth voltage or current Fourier component, or impedance, at the source (s) or load (L). The FET equivalent circuit must be described by nonlinear differential equations in the time domain. It is therefore necessary to solve (1) and (2) and the loop or node equations for the FET simultaneously.

The usual method of solving (1) and (2) consistent with the FET loop equations is to treat either the Fourier voltage or current components as variables and to use a general-purpose optimization technique to solve for them. This approach is numerically inefficient and often fails to converge. The method used here is an extension of that proposed by Kerr [7], [8] for diode mixers. It is rapidly and reliably convergent as long as the FET is stable under large-signal conditions. The essence of the method is to assume the existence of two imaginary ideal transmission lines, each an integral number of half-wavelengths long, between the FET and its source and load networks. These allow the circuit to be separated into two subnetworks, the linear source and load networks and the nonlinear FET equivalent circuit, which can be solved iteratively.

The harmonically time-varying circuit element will in general have voltage and current components at the following frequencies:

$$\omega_n = \omega_o + n\omega_p, \qquad n = \pm 1, \pm 2, \pm 3, \cdots. \tag{3}$$

Conversion matrices [9] relate the current and voltage components at different mixing frequencies in a harmonically time-varying circuit element. For a time-varying resistor, the I–V relation is the following:

$$\begin{bmatrix} V^*_{-N} \\ V^*_{-N+1} \\ \vdots \\ V_0 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} R_0 & R & \cdots & R_{-N} & \cdots & R_{-2N} \\ R_1 & R_0 & \cdots & R_{-N+1} & \cdots & R_{-2N+1} \\ \vdots & & & & & \\ R_N & R_{N-1} & \cdots & R_0 & \cdots & R_{-N} \\ \vdots & & & & & \\ R_{2N} & R_{2N-1} & \cdots & R_N & \cdots & R_0 \end{bmatrix} \cdot \begin{bmatrix} I^*_{-N} \\ I^*_{-N+1} \\ \vdots \\ I_0 \\ \vdots \\ I_N \end{bmatrix} \tag{4}$$

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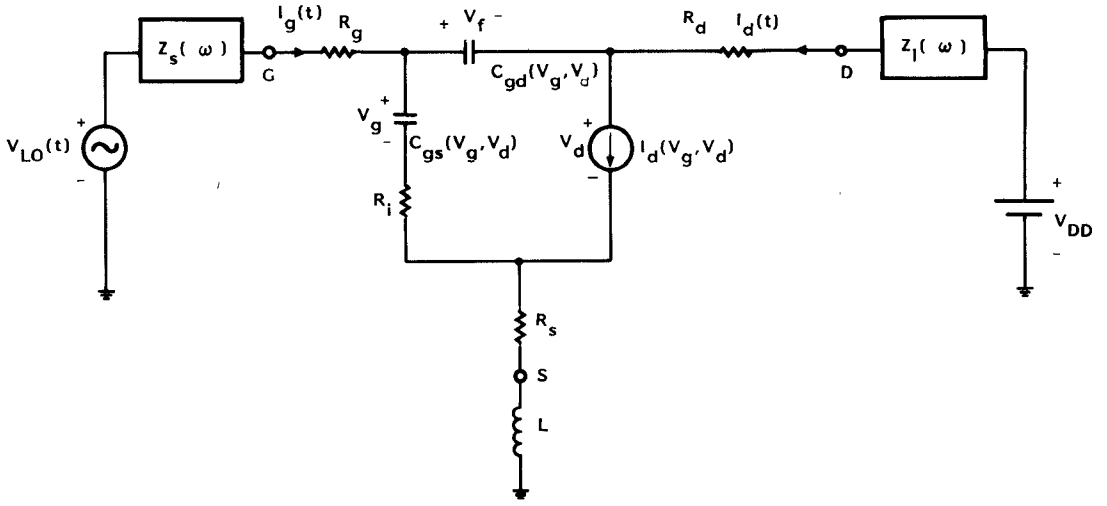

Fig. 1. Large-signal FET equivalent circuit.

where I_n and V_n are the voltages at the mixing product ω_n. The elements of the conversion matrix are the Fourier components of the time-varying resistance.

The conversion matrix for the time-varying capacitor is as follows:

$$\begin{bmatrix} I^*_{-N} \\ I^*_{-N+1} \\ \vdots \\ I_0 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} C_0\omega_{-N} & C_{-1}\omega_{-N} & C_{-2}\omega_{-N} & \cdots & C_{-2N}\omega_{-N} \\ C_1\omega_{-N+1} & C_0\omega_{-N+1} & C_{-1}\omega_{-N+1} & \cdots & \cdots \\ \vdots & \vdots & \vdots & & \vdots \\ C_N\omega_0 & C_{N-1}\omega_0 & C_{N-2}\omega_0 & \cdots & C_{-N}\omega_0 \\ \vdots & \vdots & \vdots & & \vdots \\ C_{2N}\omega_N & C_{2N-1}\omega_N & C_{2N-2}\omega_N & \cdots & C_0\omega_N \end{bmatrix} \cdot \begin{bmatrix} V^*_{-N} \\ V^*_{-N+1} \\ \vdots \\ V_0 \\ \vdots \\ V_N \end{bmatrix}. \tag{5}$$

This expression can be put into the form

$$\underline{I} = j\underset{\sim}{\Omega}\underset{\sim}{C}\underline{V} \tag{6}$$

where $\underset{\sim}{\Omega}$ is a diagonal matrix whose elements are the radian frequencies of the mixing products.

Since Kirchoff's laws hold for the frequency vectors in (4)–(6), one can write loop or node equations for the circuit of Fig. 1 in a manner analogous to that used for constant-coefficient circuits. Transfer admittances, conversion gain, and port impedances for the FET are as follows:

A. Transfer Admittance

$$\underline{I}_d = \underset{\sim}{Y}_{\text{tran}}\underline{V}_s \tag{7}$$

where

$$\underset{\sim}{Y}_{\text{tran}} = \left\{\left(\underset{\sim}{Z}_1 + \left(R_i\underset{\sim}{1} + \underset{\sim}{C}^{-1}\right)\underset{\sim}{Z}_7^{-1}\underset{\sim}{Z}_6\right)\left(\underset{\sim}{Z}_A^{-1}\underset{\sim}{Z}_B\right) + \left(R_i\underset{\sim}{1} + \underset{\sim}{C}^{-1}\right)\underset{\sim}{Z}_7^{-1}\underset{\sim}{Z}_5 + \underset{\sim}{Z}_2\right\}^{-1}$$

$$\underset{\sim}{Z}_A = \underset{\sim}{Z}_3\underset{\sim}{Z}_7^{-1}\underset{\sim}{Z}_6 + \underset{\sim}{Z}_4$$

$$\underset{\sim}{Z}_B = \underset{\sim}{R}_{\text{ds}} - \underset{\sim}{Z}_3\underset{\sim}{Z}_7^{-1}\underset{\sim}{Z}_5$$

$$\underset{\sim}{Z}_1 = \underset{\sim}{Z}_{\text{ni}} + \underset{\sim}{C}^{-1} + Lj\underset{\sim}{\Omega} + \left(R_g + R_s + R_i\right)\underset{\sim}{1}$$

$$\underset{\sim}{Z}_2 = R_s\underset{\sim}{1} + Lj\underset{\sim}{\Omega}$$

$$\underset{\sim}{Z}_3 = R_i\underset{\sim}{1} + \underset{\sim}{C}_r^{-1} + \left(\underset{\sim}{1} + \underset{\sim}{R}_{\text{ds}}\underset{\sim}{G}_m\right)\underset{\sim}{C}^{-1} + \underset{\sim}{R}_{\text{ds}}$$

$$\underset{\sim}{Z}_4 = R_i\underset{\sim}{1} + \left(\underset{\sim}{1} + \underset{\sim}{R}_{\text{ds}}\underset{\sim}{G}_m\right)\underset{\sim}{C}^{-1}$$

$$\underset{\sim}{Z}_5 = \underset{\sim}{Z}_{\text{no}} + Lj\underset{\sim}{\Omega} + \underset{\sim}{R}_{\text{ds}} + \left(R_d + R_s\right)\underset{\sim}{1}$$

$$\underset{\sim}{Z}_6 = R_s\underset{\sim}{1} + Lj\underset{\sim}{\Omega} - \underset{\sim}{R}_{\text{ds}}\underset{\sim}{G}_m\underset{\sim}{C}^{-1}$$

$$\underset{\sim}{Z}_7 = \underset{\sim}{R}_{\text{ds}}\left(\underset{\sim}{G}_m\underset{\sim}{C}^{-1} + \underset{\sim}{1}\right)$$

where $\underset{\sim}{R}_{\text{ds}}$ is the conversion matrix for $r_{\text{ds}}(t)$, $\underset{\sim}{G}_m$ is the conversion matrix for $g_m(t)$, $\underset{\sim}{C}$ is the conversion matrix for $C_{\text{gs}}(t)$, $\underset{\sim}{C}_r$ is the conversion matrix for $C_{\text{gd}}(t)$, $\underset{\sim}{Z}_{\text{ni}}$ is the source impedance matrix; $\underset{\sim}{Z}_{\text{ni}} = \text{diag}(Z_s(\omega_n))$, $\underset{\sim}{Z}_{\text{no}}$ is the load impedance matrix; $\underset{\sim}{Z}_{\text{no}} = \text{diag}(Z_L(\omega_n))$, $\underset{\sim}{\Omega}$ is the diagonal frequency component matrix as described in (6), $\underset{\sim}{1}$ is the identity matrix, $\underline{V}_s$ is the excitation vector (usually $\underline{V}_s$ has only one nonzero element, the input voltage source), and $\underline{I}_{\text{d}}$ is the drain current vector. Scalar quantities are defined in Fig. 1.

B. Conversion Gain, $G_t(\omega_m, \omega_n)$

ω_n is the input frequency as defined in (1), ω_m is the output frequency as defined in (1), and

$$G_t(\omega_m,\omega_n) = 4\left|\underset{\sim}{Y}_{\text{tran}}(m,n)\right|\text{Re}\left\{Z_{\text{ni}}(\omega_n)\right\}\text{Re}\left\{Z_{\text{no}}(\omega_m)\right\}. \tag{8}$$

C. Input Impedance with the Output Terminated

$$\underset{\sim}{Z}_{\text{in}} = \underset{\sim}{Z}_1 + \left(\underset{\sim}{Z}_2 + \left(R_i\underset{\sim}{1} + \underset{\sim}{C}^{-1}\right)\underset{\sim}{Z}_7^{-1}\underset{\sim}{Z}_5\right)\underset{\sim}{Z}_B^{-1}\underset{\sim}{Z}_A + \left(R_i\underset{\sim}{1} + \underset{\sim}{C}^{-1}\right)\underset{\sim}{Z}_7^{-1}\underset{\sim}{Z}_6 - \underset{\sim}{Z}_{\text{ni}}. \tag{9}$$

$\underset{\sim}{Z}_{\text{in}}$ is defined by the relation

$$\underline{V}_{\text{gs}} = \underset{\sim}{Z}_{\text{in}}\underline{I}_g$$

where $\underline{V}_{gs}$ and $\underline{I}_g$ are the gate-to-source voltage vector and gate current vector, respectively. All other matrices are as defined in Section II*A*.

D. Output Impedance with the Input Terminated

$$\underline{Z}_{out} = \left(\underline{Z}_5 + \underline{Z}_7\underline{R}^{-1}\underline{Z}_2\right) + \left(\underline{Z}_6 + \underline{Z}_7\underline{R}^{-1}\underline{Z}_1\right)\left(\underline{Z}_4 - \underline{Z}_3\underline{R}^{-1}\underline{Z}_1\right)^{-1} \left(\underline{R}_{ds} + \underline{Z}_3\underline{R}^{-1}\underline{Z}_2\right) - \underline{Z}_{no} \quad (10)$$

where

$$\underline{R} = R_i\underline{1} + \underline{C}^{-1}.$$

All other vectors are as defined in Section II*A*.

$\underline{Z}_{out}$ is defined by the relation

$$\underline{V}_{ds} = \underline{Z}_{out}\underline{I}_d$$

where $\underline{V}_{ds}$ and $\underline{I}_d$ are the drain-to-source voltage vector and drain current vector, respectively.

III. FET Characterization

A major concern in this work is the characterization of the FET. In principle, one can determine the voltage dependences for the circuit elements in Fig. 1 by fitting to *S* parameters measured at a number of different bias levels. This approach is prohibitively laborious for practical design purposes and cannot be used for monolithic circuits where FET *S*-parameter data may not be available *a priori*.

The FET characterization used here is derived primarily from the model of Pucel [10], with some modifications to improve the agreement between calculated and measured *I–V* characteristics. The modification involves an improved estimate of the voltage drop in the velocity-saturated region of the FET channel, where a charge domain forms. The parameters of this model are fit to measured *I–V* data. Resistances which do not affect the dc *I–V* characteristic are obtained from *S* parameters measured at one bias level, and capacitances are obtained by integrating over the gate depletion region. Hence, the FET is completely described by the parameters of the model and the values of the fixed elements of the equivalent circuit, a total of only ten parameters.

A comparison of measured and calculated *I–V* characteristics for an Avantek AT8251 FET are presented in Fig. 2. The measured gate–source capacitance is presented in Fig. 3, along with the calculated capacitance of a simple Schottky barrier junction. The measured gate–drain capacitance is presented in Fig. 4. This data shows that the often-used Schottky-barrier junction assumption for C_{gs} and the constant capacitance assumption for C_{gd}, are valid only as long as the FET remains in its saturation region. This model will be described in a subsequent paper.

IV. FET Mixer Design and Performance

Two FET mixers were designed for operation at 8.2 GHz with 1.2-GHz IF and 7.0-GHz LO. The first was used primarily to verify the theory, although its performance was optimized. It was designed for a single frequency; i.e., it was not intended to operate over a bandwidth. Its performance was found to be uniform, however, over approximately 100 MHz. It was possible to disassemble it and to measure the embedding impedances (the source and load impedances seen at the FET drain and gate ($Z_L(\omega_n)$ and $Z_s(\omega_n)$, respectively). The second mixer was designed using the above theory but was not disassembled to measure its embedding impedances. It did, however, achieve the

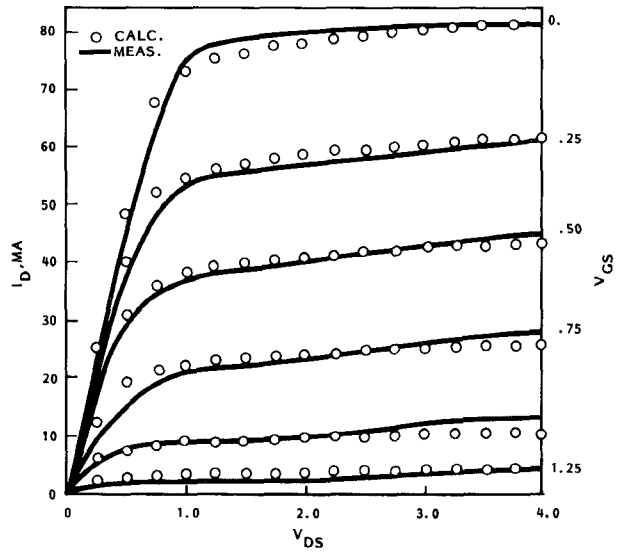

Fig. 2. AT8251 measured and modeled *I–V* characteristic. Solid lines are measured, crosses are calculated.

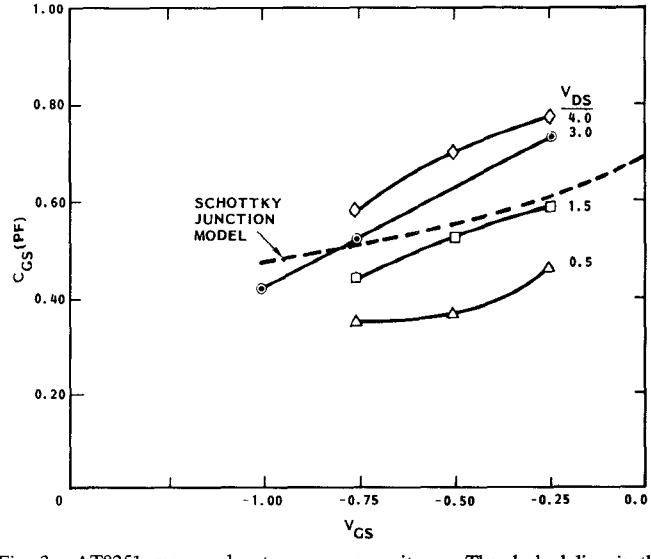

Fig. 3. AT8251 measured gate–source capacitance. The dashed line is the capacitance obtained by use of a Schottky-barrier junction capacitance model.

predicted conversion gain of 6 dB at full LO level and required very little tuning. It was intended to achieve good performance over a 500-MHz bandwidth. The first mixer uses an unpackaged Avantek AT8251 FET; the second, a packaged Avantek AT8060. State-of-the-art performance was achieved with both mixers.

The matching circuits short circuit all LO harmonics and mixing products other than the IF at the FET drain and the signal and LO fundamental at the input. These terminations prevent spurious responses and downconversion of input noise at higher order mixing frequencies. Optimum noise figure was achieved with the input matched at the signal frequency. The IF output impedance is dominated by the average value of $R_{ds}(t)$, and therefore rises sharply as the LO level is raised past the point where the gate voltage reaches pinchoff at negative peaks. It is consequently very difficult to match an FET mixer IF over any but a narrow bandwidth; the high load impedance required may give too much gain or cause instability. The goal of IF circuit design is therefore to present an appropriate real impedance to the drain of the FET at the IF frequency. The result is a high IF

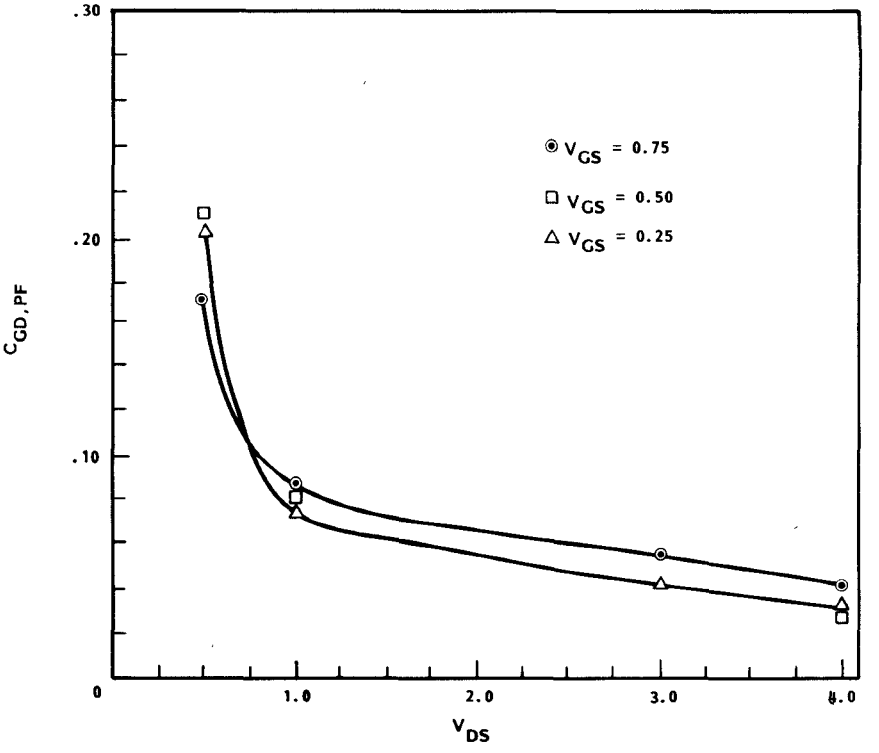

Fig. 4. AT8251 measured gate–drain capacitance.

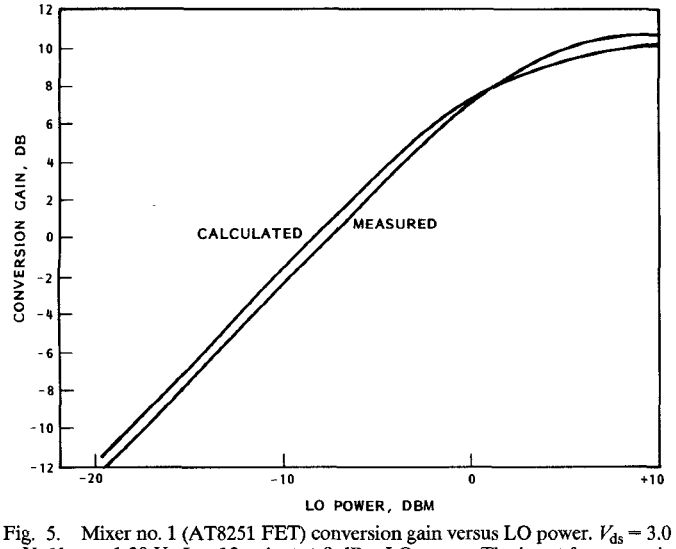

Fig. 5. Mixer no. 1 (AT8251 FET) conversion gain versus LO power. $V_{ds} = 3.0$ V, $V_{gs} = -1.30$ V. $I_d = 12$ mA at +9-dBm LO power. The input frequency is 8.2 GHz with a 7.0-GHz LO and 1.2-GHz IF.

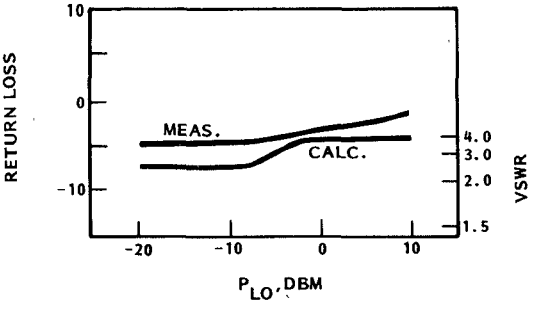

Fig. 6. Calculated and measured output VSWR for the AT8251 mixer versus LO power, for an IF load impedance of 70 Ω, real. The IF frequency is 1.2 GHz.

VSWR, which can be lowered if necessary by using isolators or balanced structures. For both mixers described here, the IF load impedance is approximately 70 Ω.

The matching circuits for these mixers were realized in microstrip on 0.025-in alumina substrates. They consist of simple series transmission lines and open-circuit stubs. The input IF short was realized with a shorted stub one-quarter wavelength long at the signal frequency. The output network is a low-pass structure using series high- and low-impedance lines.

Fig. 5 presents a comparison of measured and calculated conversion gains for the first mixer. These show excellent agreement over the entire range of LO power.

The input impedance of the first mixer at full LO excitation was calculated to be $4-j39$ and the measured embedding impedance is $4+j36$. Considering that some of this error is caused by small circuit losses and the difficulty of the measurement, the agreement is remarkably good. The measured and calculated output VSWR is shown in Fig. 6; the agreement is reasonably good. The major cause of error is the frequency sensitivity of R_{ds}; it is much lower at microwave frequencies than is indicated at dc by $I-V$ curves.

The first mixer has a minimum SSB noise figure of 5.6 dB, which is flat to 0.1 dB over a remarkably wide LO power range, 7 dB. The intercept point for third-order intermodulation products is +15 dBm. The noise figure is optimum below +3-dBm LO power, and the intercept point is optimum at +9 dBm. However, the noise figure rises only 0.5 dB at +9 dBm. All these data were obtained with the same bias voltages and tuning, 3.0-V drain bias and −1.3-V gate bias. The gate bias voltage is very close to pinchoff.

The second mixer has lower gain, primarily because the gate width of the AT8060 is half that of the AT8251 (300 versus 600 μm), and its transconductance swing is therefore approximately half, as well. Its gain, noise figure, and third-order intercept point are summarized in Figs. 7–9. The dc drain and gate biases are 3.0

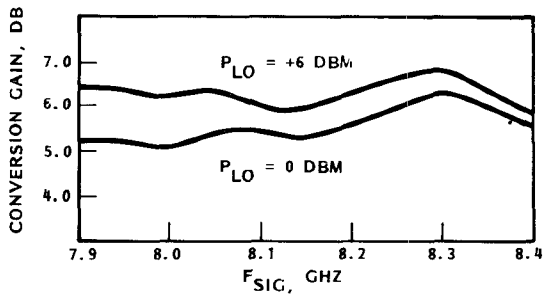

Fig. 7. Gain of Mixer no. 2 (AT8060 FET). The LO level for optimum noise figure is 0 dBm; optimum third-order intermodulation is +6 dBm. $V_{ds} = 3.0$ V, $V_{gs} = -1.0$ V.

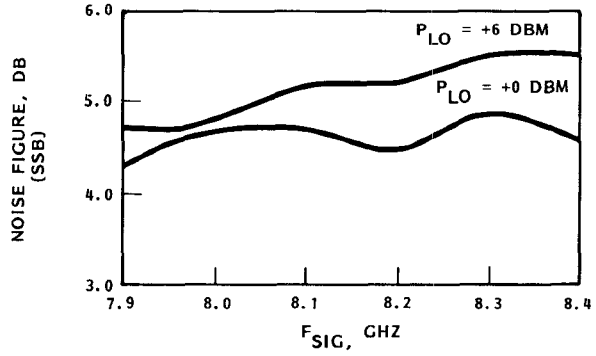

Fig. 8. Noise figure of Mixer no. 2 at the LO level for optimum noise (0 dBm) and optimum intermodulation (+6 dBm). DC bias for both cases is $V_{ds} = 3.0$ V, $V_{gs} = -1.0$ V.

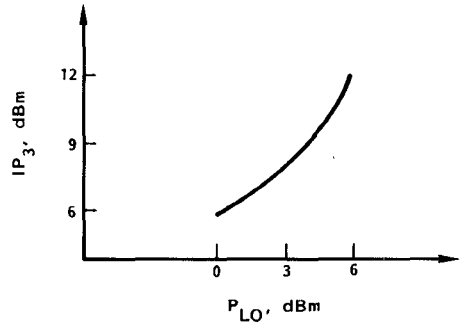

Fig. 9. Third-order intermodulation intercept point of mixer no. 2, as a function of LO level. DC bias is the same as that used for noise figure data.

and −1.0 V, respectively. As with the first mixer, the gate is biased close to pinchoff.

It is worthwhile to compare these results to the performance of diode mixers. Commercially available balanced diode mixers used most often in the microwave range exhibit conversion losses of 5–9 dB, third-order intercept points (output) of 0–13 dBm, and have LO power requirements of 8–18 dBm. It is possible in some cases to achieve mixer noise figures as low as 3.5 dB by narrow-band design and image enhancement, and receiver noise figures around 5 dB. Such mixers require considerable effort to design and optimize, and will almost certainly be single-ended structures with relatively poor intermodulation performance. Multidiode balanced mixers offer better intermodulation performance, approaching that of FET mixers, at the expense of high LO power requirements. However, most balanced structures cannot be tuned and optimized as effectively as single diode mixers, so their noise performance is usually worse. The FET mixer offers lower noise and equal or better linearity with less LO power. It can be incorporated into balanced structures for even lower intermodulation without sacrificing noise performance or creating a terrifying design problem.

V. Conclusions

A very general theory of active mixers has been presented, with application to GaAs FET mixers. The theory has been validated experimentally.

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Microwave Hyperthermic Distributions in a Layered Living Body with Nonlinear Thermoregulatory Properties

S. CAORSI

***Abstract*—In this paper, the microwave heating of biological systems with nonlinear thermoregulatory properties is considered. Temperature distributions are calculated in a layered biological model exposed to uniform plane waves. The external surfaces of such a model are cooled and its thermoregulatory properties are assumed to be nonlinear functions of the local temperature. The calculation of the space-time evolution of the temperature is performed using a numerical program that has been developed by applying the finite-difference method. In this numerical program, the nonlinear thermoregulatory functions are given either by a segment-linearization process or by an arbitrary analytical form or by a transformation of an input sample set. The mean power density of the incident electromagnetic wave and the coolant temperature are also taken time-dependent.**

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The author is with the Biophysical and Electronic Engineering Department, University of Genoa, Via all'Opera Pia, lla, 16145, Genova, Italy.